UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

JS

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/411,698	10/01/99	STOLOWITZ M	44541/212

LM01/0726

003528
STOEL RIVES
STANDARD INSURANCE CENTER
900 SW FIFTH AVENUE, SUITE 2300
PORTLAND OR 97204-1268

EXAMINER	
DU, T	

ART UNIT	PAPER NUMBER
2782	6

DATE MAILED: 07/26/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/411,698	STOLOWITZ, MICHAEL C.	
	Examiner	Art Unit	
	Thuan N. Du	2782	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *23 May 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☒ The proposed drawing correction filed on *23 May 2000* is: a)☒ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

1. This response to amendment filed on May 23, 2000 (paper no. 5).

2. Applicant's arguments with respect to claims 1-19 have been considered but are mood in view of the new ground(s) rejection.

3. Claims 1-19 are presented for examination.

Drawings

4. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on May 23, 2000 have been approved by the examiner.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Searby (U.S. Patent No. 5, 765,186).

7. As per claim 1, Searby teaches a method of reading data from a RAID array of disk drives comprising the steps of:

providing a single buffer memory having a data port coupled to all of the disk drive data ports for transferring digital data [Fig. 2, buffers 37-40. Considering the set of buffers 37-40 is a single bigger buffer with plurality of locations, e.g. locations 37-40];

providing a single address counter for addressing consecutive locations in the buffer memory [col. 7, lines 20-24. Inherently, the controller provides a single address counter for addressing the locations of the buffer stated above];

sending read commands to all of the disk drives so as to initiate read operations in all of the disk drives [col. 6, lines 27-31];

waiting until read data elements are ready at all of the disk drive data ports [col. 6, lines 64-67];

after read data elements are ready at all of the disk drive data ports, synchronously retrieving and storing the read data elements from all of the read drive data ports into consecutive locations in the buffer memory under addressing control of the single address counter [col. 6, line 64 through col. 7, line 10];

wherein said synchronously retrieving and storing the read data elements from all of the read drive data ports includes clocking the read data through a common pipeline so as to form a

contiguous word serial data stream through the pipeline [Fig. 3, shift register 57, col. 9, lines 40-42];

concurrently computing redundant data from the read data while the read data moves through the pipeline [col. 9, lines 40-60];

and, if a failed disk drive has been identified, substituting the computed redundant data into the word serial data stream in lieu of the failed disk drive data [col. 9, lines 50-55]; and

storing the word serial data stream into the buffer memory thereby providing the requested read data without incurring delay to reconstruct data stored on the failed disk drive [col. 4, lines 29-44].

Searby does not explicitly teach the step of providing a series of registers forming a common pipeline disposed in between the disk drive data ports and the buffer memory data ports. Official Notice is taken that it is well known to use a series of registers to form a common pipeline and it is a matter of design choice to dispose the pipeline in between the disk drive data ports and the buffer memory data ports.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose the pipeline formed by series of shift registers in between the disk drive data ports and the buffer memory data ports to transfer data through the pipeline (for reconstructing data, for example) before the data reaches the buffer to enhance the error checking and data reconstructing of Searby's system.

8. As per claim 2, Searby teaches the system comprising:

host bus interface means for interfacing to a host bus data transfer [register 50 in Figs. 2, 3 is in the form of host bus interface means];

buffer memory means for storing data [Figs. 2, 3, buffers 37-40];

a processor for controlling operation of the disk controller so as to effect synchronous data transfers between the buffer memory and an array of disk drives [Figs. 2, 3, controller 51];

disk drive interface means including a drive data bus for interfacing the controller to an array of disk drives including a redundant drive [Figs. 2, 3, interfaces 25-28];

redundant data operating means for forming redundant drive data on the fly [parity generator 55 of Fig. 3 is in the form of redundant data operating means].

Searby does not explicitly teach the redundant data operating means disposed along the drive data bus between the buffer memory and the drives. But it is the matter of design choice to place the redundant logic in between the buffer memory and the drives for forming redundant drive data as data passes from the buffer to the drives.

9. As per claim 3, Searby teaches the redundant data operating means includes:

a multiplexer having a first input coupled to the buffer memory port to receive write data [parity generator 55 is in the form of the multiplexer];

an XOR/LOAD circuit having a first input coupled to the buffer memory port [col. 9, lines 5-8];

an accumulator coupled to the output of the XOR/LOAD circuit [col. 9, lines 8-11];

a feedback path from the accumulator circuit to a second input of the XOR/LOAD circuit [col. 9, lines 15-23];

the multiplexer having a second input coupled to the accumulator [the accumulator is considered same circuit with the multiplexer]; and

the multiplexer output coupled to the drive data bus for interfacing to the array of disk drives, so that in operation the multiplexer selects either a word of write data from the buffer memory for writing to disk, or a redundant word formed in the accumulator for writing to disk as redundant data [col. 9, lines 8-23].

10. As per claim 4, Searby discloses a second redundant data operating means for reconstructing missing data [data generator 56 and delay shift register 57 of Fig. 3].

11. As per claim 5, Searby teaches the second redundant data operating means includes:

a pipeline of register through which read data is passed during a disk read operation [delay shift register 57 of Fig. 3];

an input end of the pipeline coupled to the disk drive data bus to receive read data [Fig. 3];

a multiplexer having a first input coupled to an output end of the pipeline to receive read data [register 50 is also in the form of the multiplexer];

an XOR circuit coupled to the disk drive data bus to receive read data [data generator 56 of Fig. 3, col. 9, lines 42-43];

an accumulator having an input coupled to XOR circuit output [data generator 56 of Fig. 3, col. 9, lines 54-55];

the multiplexer selects either a word of valid read data from the pipeline or a reconstructed word formed in the accumulator in lieu of missing or bad data [col. 9, lines 48-60].

Searby does not explicitly teach:

a holding circuit having an input coupled to the XOR circuit output;

a holding circuit having an input coupled to the accumulator to hold accumulated data;

a feedback path from the output of the accumulator to a second input of the XOR circuit for forming XOR data in the accumulator as valid read data passes through the XOR circuit from the drive data bus;

an output path from the hold circuit to a second input of the multiplexer to provide reconstructed missing data.

Searby teaches the delay circuit to hold the output data while the calculating of missing data is performing. It would have been obvious to one of ordinary skill in the art to have a hold circuit coupled to the data generating circuit to hold the calculated data before the data input to the multiplexer by the output path of the hold circuit.

12. As per claim 6, Searby teaches the system comprising:

a buffer memory [Figs. 2, 3, buffers 37-40];

disk drive interface means for connection to a plurality of disk drives [Figs. 2, 3, interfaces 25-28];

control means coupled to the buffer memory and coupled to the data bus for synchronously transferring data over the data bus between the buffer memory and the interface means [controller 51 of Figs. 2, 3, col. 6, line 64 to col. 7, line 1];

means for generating redundant check data on the fly during execution of disk write operation [parity generator 55 of Fig. 3].

Searby does not explicitly teach the means for generating redundant check is disposed between the buffer and the data bus. But it is the matter of design choice to place the generating means between the buffer memory and the data bus for generating redundant check during execution of a disk write operation.

13. As per claims 7-9, Searby teaches the system comprising:

a buffer memory [Figs. 2, 3, buffers 37-40];

disk drive interface means for connection to a plurality of disk drives [Figs. 2, 3, interfaces 25-28];

control means coupled to the buffer memory and coupled to the data bus for synchronously transferring data over the data bus between the buffer memory and the interface means [controller 51 of Figs. 2, 3, col. 6, line 64 to col. 7, line 1];

means for reconstructing missing data during a read operation [data generator 56 and delay shift register 57 of Fig. 3].

Searby does not explicitly teach the means for reconstructing missing data is disposed between the buffer and the drive data bus. But it is the matter of design choice to place the reconstructing means between the buffer memory and the drive data bus for reconstructing missing data during a read operation.

14. As per claims 10-19, they are the corresponding method steps of claimed apparatus. Therefore, they are rejected under the same rational.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (703) 308-6292. The examiner can normally be reached on Monday-Friday: 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Thuan N. Du
July 14, 2000

THOMAS C. LEE
SUPERVISORY PATENT EXAMINER
GROUP 2700